Fig. 1
PRIOR ART

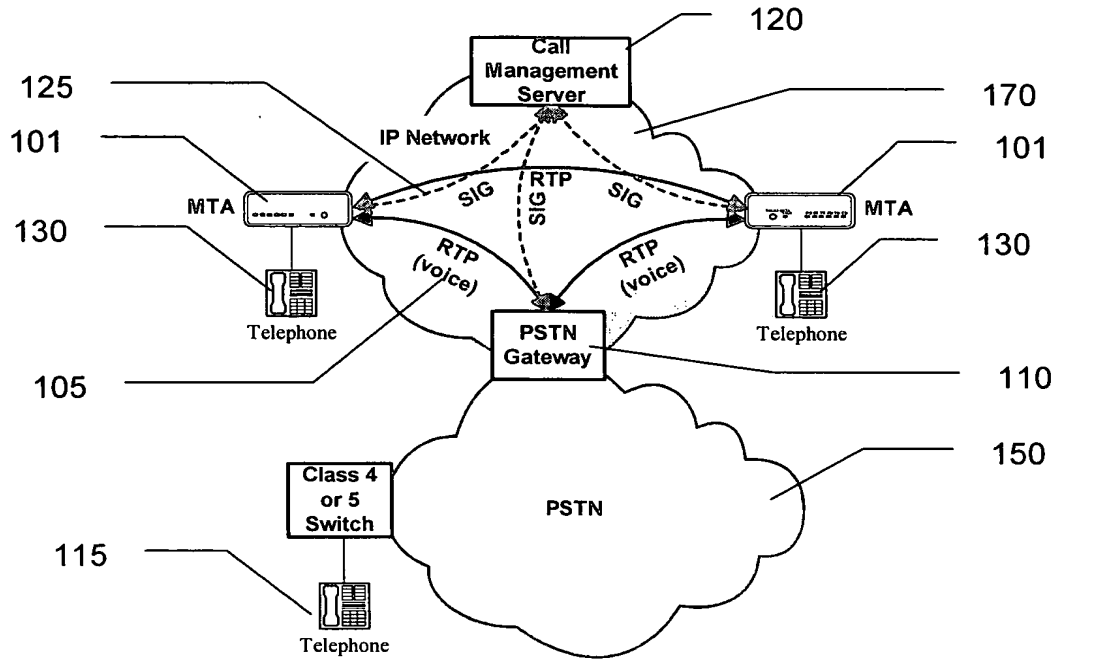


Fig. 2

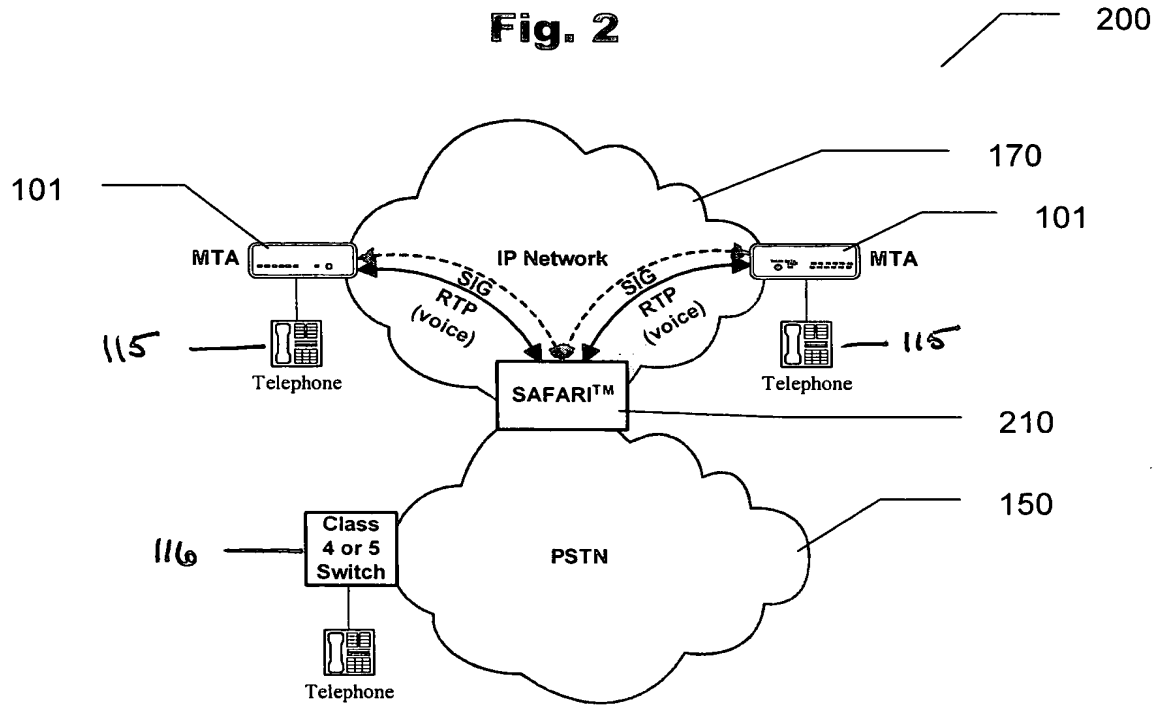


Fig. 3

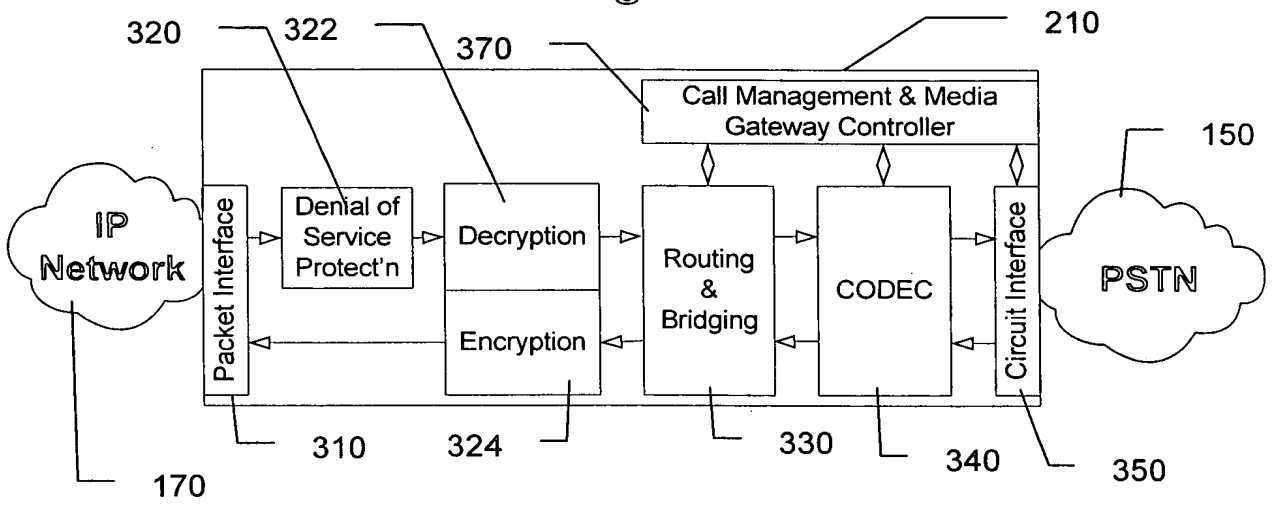


Fig. 4A

Ingress Flow

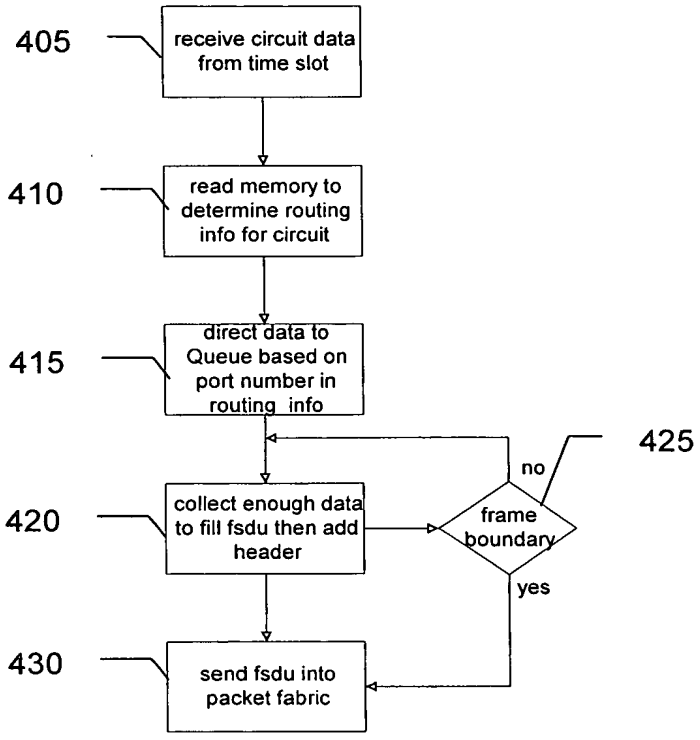


Fig. 4B

Egress Flow

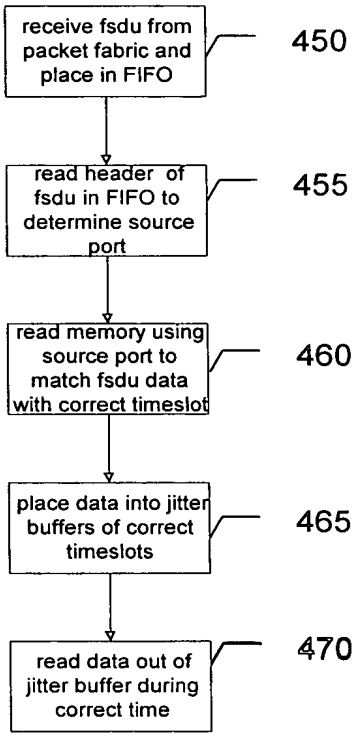
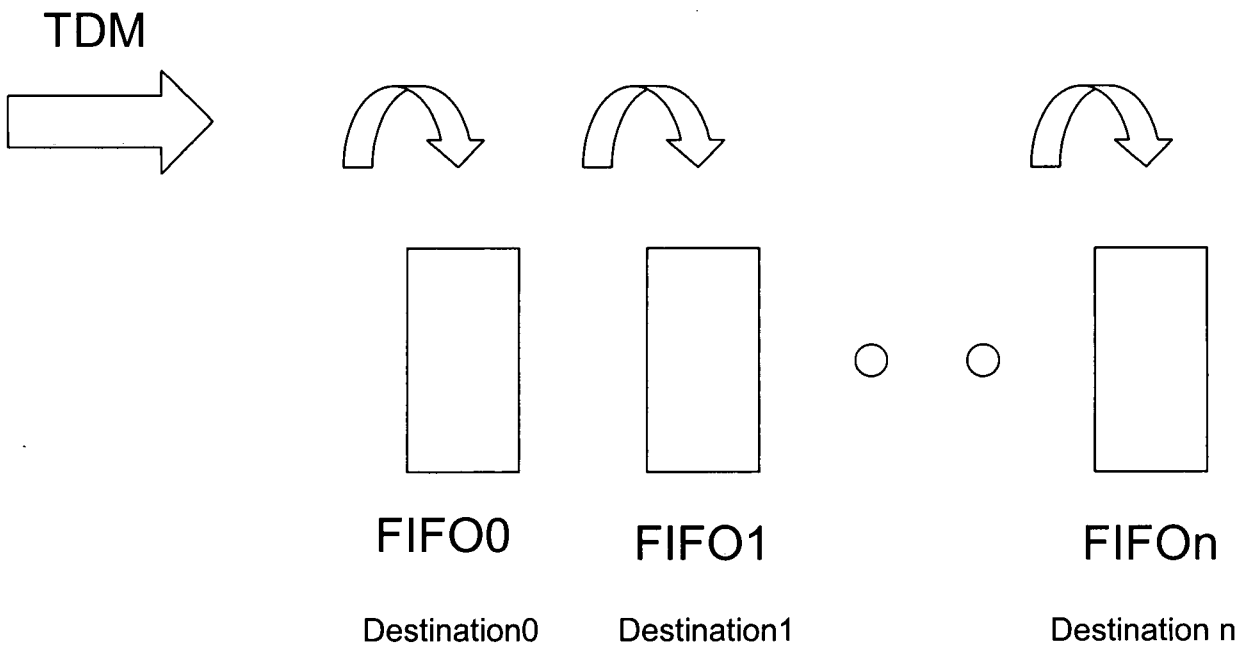


Figure 4C



9000783

Fig. 5

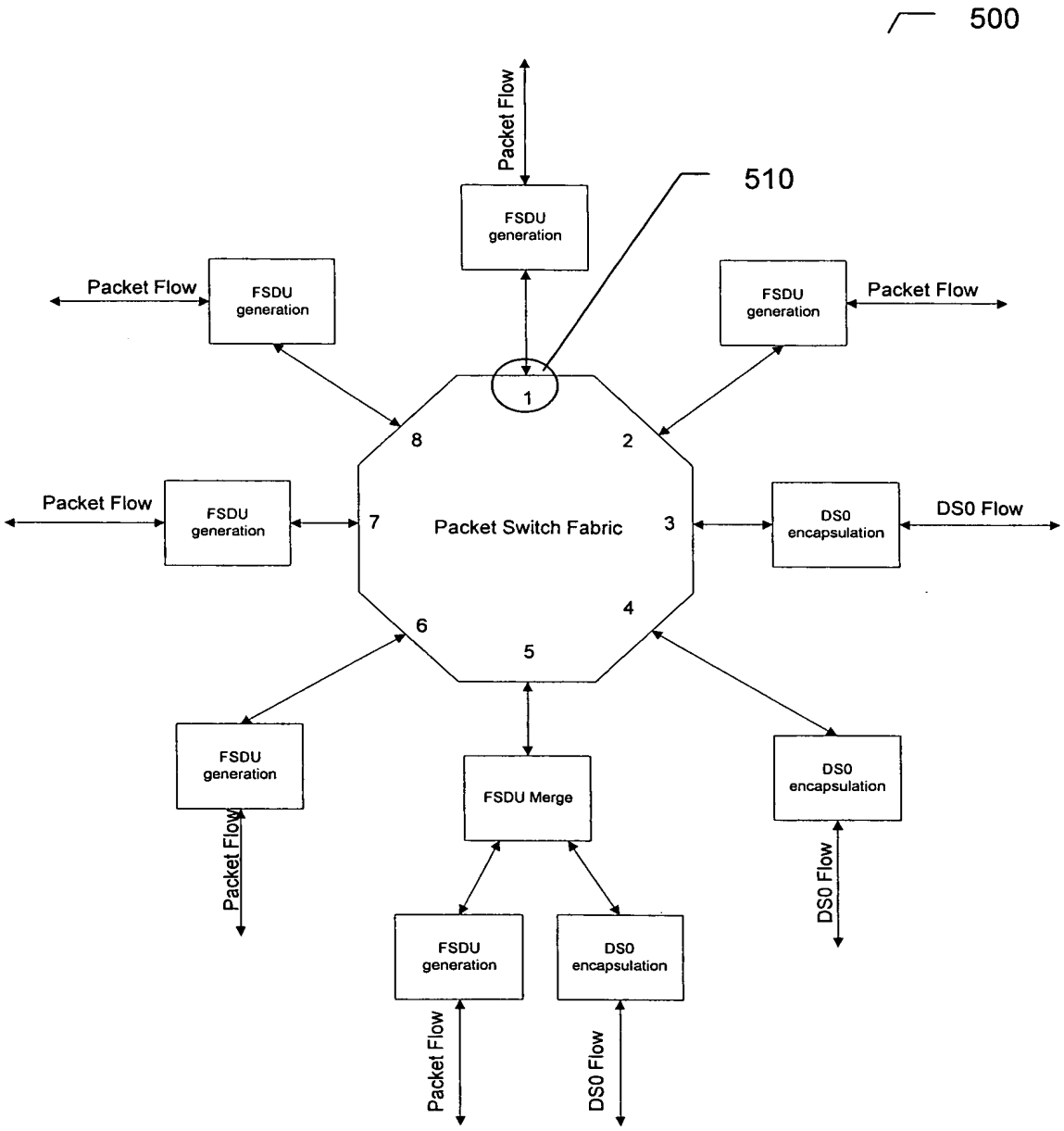

500
510
Packet Flow
FSDU generation
Packet Flow
FSDU generation
FSDU generation
Packet Flow
1
8
2
Packet Flow
FSDU generation
7
Packet Switch Fabric
3
DS0 encapsulation
DS0 Flow
4
6
5
FSDU generation
FSDU Merge
DS0 encapsulation
Packet Flow
DS0 Flow
FSDU generation
DS0 encapsulation
Packet Flow
DS0 Flow

Fig. 6

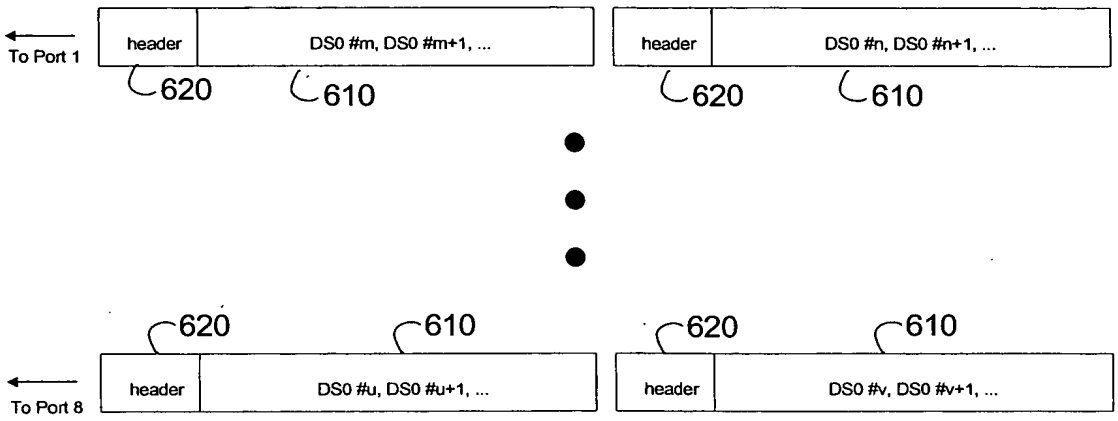
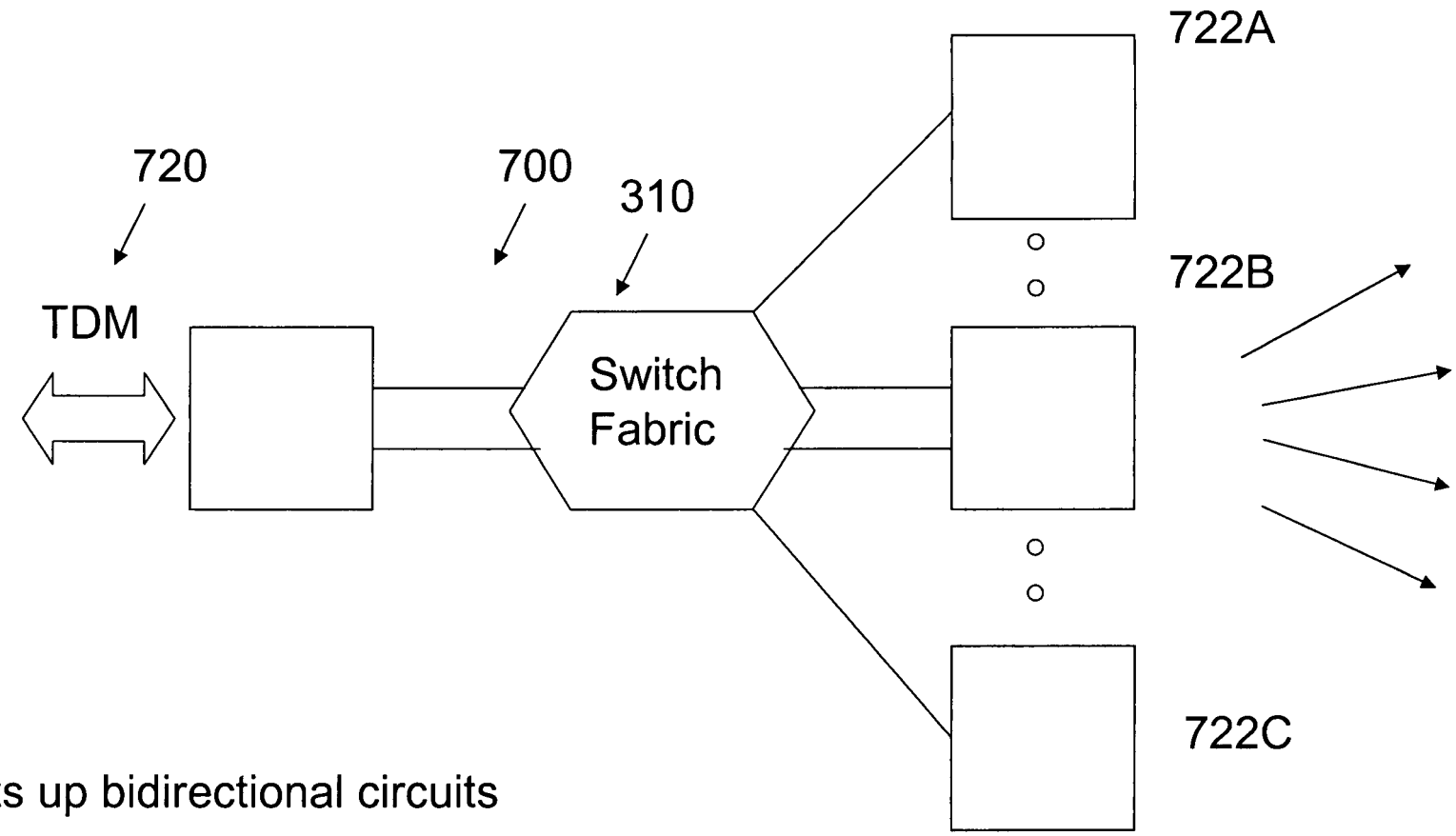

To Port 1
header
DS0 #m, DS0 #m+1, ...
620
610
header
DS0 #n, DS0 #n+1, ...
620
610
620
610
620
610
To Port 8
header
DS0 #u, DS0 #u+1, ...
header
DS0 #v, DS0 #v+1, ...

Figure 7



Sets up bidirectional circuits

Figure 8


Control Cell$_1$
Control Cell$_0$
Routing Header

OR


Control Cell$_1$
Control Cell$_1$
Routing Header$_1$
Control Cell$_0$
Routing Header$_0$